GR 98 P 8041

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Thomas Huttner

RCE of Applic.: 09/313,424 filed on May 17, 1999

RCE filed : November 12, 1999

Title : SOI Semiconductor Configuration And Method Of Fabricating The Same

Examiner : Brook Kebede

Group Art Unit : 2823

P R E L I M I N A R Y A M E N D M E N T

S i r :

Responsive to the *Advisory Action* dated September 4, 2002, and in view of the attached *Request for Continued Examination* (RCE), kindly amend the above-identified application as follows:

In the Claims:

Claim 16 (amended). A method of fabricating a semiconductor configuration, which comprises the following steps:

E1 fabricating a semiconductor structure having a base layer, an insulation layer, a monocrystalline silicon layer, and an interface between the insulation layer and the monocrystalline silicon layer;